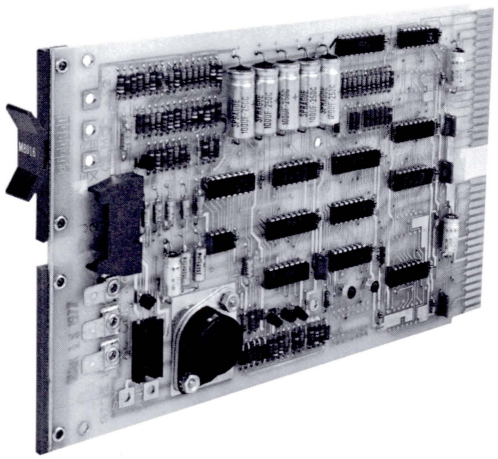
DIGITAL EQUIPMENT CORPORATION

MODULE DATA SHEET

LOGIC PRODUCTS

NOVEMBER 1977

KPV11 Power Fail/Line Time Clock Generator Module



DESCRIPTION

The KPV11 is an LSI-11 power fail/line time clock (LTC) generator. It is compatible with all LSI-11 component systems and LSI-11 backplane options. The KPV11 module is designed for installation in any LSI-11 bus-structured backplane or remote installation (not installed in a backplane) via an optional cable which connects the option to the LSI-11 backplane. An optional console panel (DEC Part No. 54-11808) is available for manual control of LTC and power signal generation and display of dc power on/off status and processor run/halt state. KPV11 options and LSI-11 system functions are shown in Figure 1.

FEATURES

- Automatic generation of BPOK and BDCOK power-up/power-down signal sequence.
- Automatic program restoration and starting when used with non-volatile memory and appropriate software routines.
- Built-in line time clock is program compatible with the UNIBUS option KW11-L line time clock (refer to PDP-11 Peripherals Handbook for description). The KPV11 is factory-configured for Line clock Status (LKS) register address and operations.
- Line time clock time reference can be provided by a signal source (user supplied) other than the power line.
- Optional termination resistor packs allow the KPV11 to function as a bus terminator module when plugged into an LSI-11 bus-structured backplane.

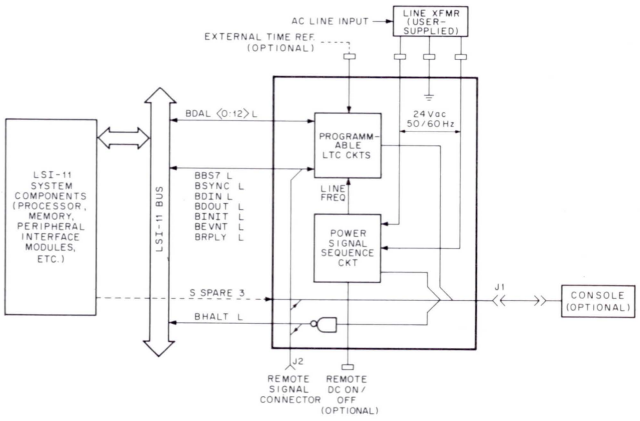


Figure 1. KPV11 System Functions

- Can be installed in the LSI-11 backplane or mounted remotely. An optional cable connects the KPV11 to the LSI-11 backplane when mounted remotely.
- Expandable with the 54-11808 console panel option.
- Contained on a single 13.2 cm (5.2 in.) by 22.8 cm (8.9 in.) module. (Double height, extended length.)

The following presents KPV11 specifications and information for configuring, installing, programming, operating, and maintaining the option.

SPECIFICATIONS

Mechanical

	Dimensions
Height—double height:	13.2 cm (5.2 in.)
Width —single width:	1.27 cm (0.5 in.)
Length—extended length:	22.8 cm (8.9 in.)

Environmental

Operating temperature:	5°C to 50°C (41°F to 122°F)
Relative humidity:	10% to 95% (no condensation)

Electrical

Power requirements:
AC line voltage monitor input: 24 Vac with grounded center tap ±10%, DC operating power: +5 V ±5%, 560 mA.

OPTIONS

Model/Part No.	Description
54-11808	Console panel (P.C. assembly)
70-11656	Console bezel
70-12754	Remote signal cable
70-08612	Console signal/power cable

Power Signal Sequence Timing

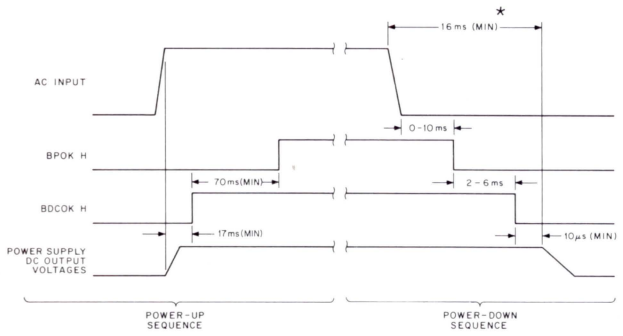


Figure 2. Power Signal Sequence Timing

***26 ms minimum hold-up time is required of the power supplies used with the KPV11 option.**

LSI-11

Backplane Pin Utilization

Module Side 1 (Component Side)

Row A Pin	Signal Mnemonic	Row B Pin	Signal Mnemonic
AA1	BSPARE1	BA1	BDCOK H
AB1	BSPARE2	BB1	BPOK H
AC1	BAD16 L	BC1	SSPARE4
AD1	BAD17 L	BD1	SSPARE5
AE1	SSPARE1	BE1	SSPARE6
AF1	SSPARE2	BF1	SSPARE7
AH1	SSPARE3	BH1	SSPARE8
AJ1	GND	BJ1	GND
AK1	MSPAREA	BK1	MSPAREB
AL1	MSPAREA	BL1	MSPAREB
AM1	GND	BM1	GND
AN1	BDMR L	BN1	BSACK L
AP1	BHALT L	BP1	BSPARE6
AR1	BREF L	BR1	BDVNT L
AS1	PSPARE3	BS2	PSPARE4
AT1	GND	BT1	GND
AU1	PSPARE1	BU1	PSPARE2
AV1	+5B	BV1	+5B

Module Side 2 (Solder Side)

Row A Pin	Signal Mnemonic	Row B Pin	Signal Mnemonic
AA2	+5	BA2	+5
AB2	−12	BB2	−12
AC2	GND	BC2	GND
AD2	+12	BD2	+12
AE2	BDOUT L	BD2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	BWTBT L	BK2	BDAL6 L
AL2	BIRQ L	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDALO L	BU2	BDAL14 L
AV2	BDALI L	BV2	BDAL15 L

Connector Pin Assignments

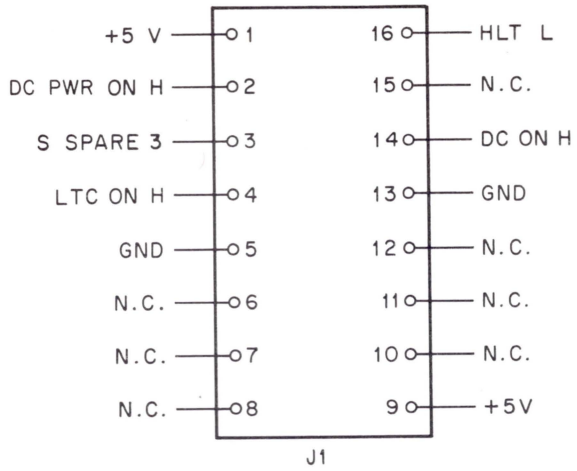


Figure 3. Remote Console Connector (J1)

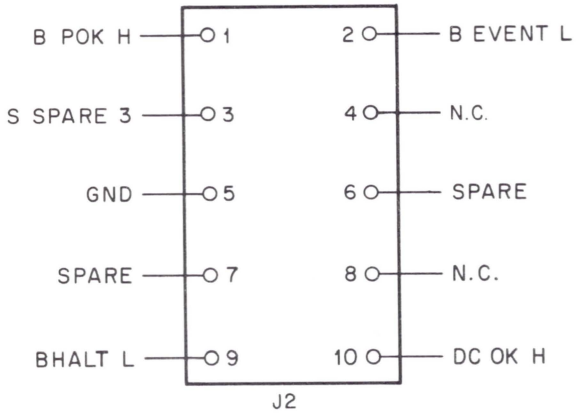


Figure 4. Backplane Signal Connector (J2)

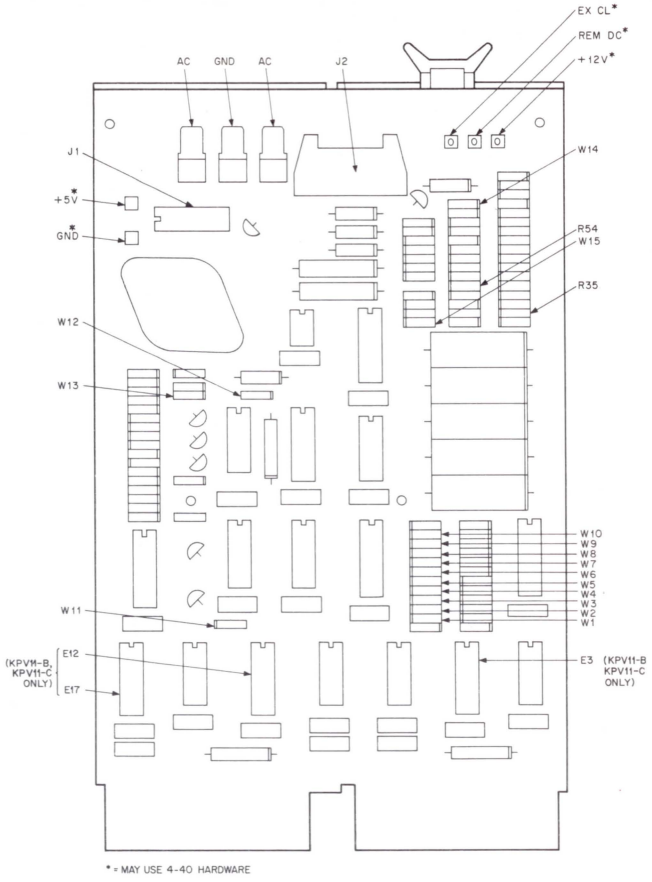


Figure 5. KPV11 Jumper, Connector, and Pad Locations

***May use 4-40 Hardware**

CONFIGURING LTC JUMPERS

LTC jumpers are located on the KPV11 module as shown in Figure 5 and are factory-configured for programmable operation with the LKS (Line clock Status) register address (177546) as shown in Figure 6. Normally, it will not be necessary to reconfigure LTC jumpers; however, it is possible to alter LTC operation as listed below and the LKS device address as shown in figure 6.

Jumper	Installed	Removed
W12	Enable manual control or continuous LTC interrupt request operation. Do not install when W13 is installed.	*Disable continuous or manual operation.
W13	*LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.	LTC interrupt requests cannot be program controlled.
W14	*Console (optional) LTC ON/OFF switch enabled.	Console LTC ON/OFF switch disabled.
W15	*LTC signal occurs at the power line frequency.	LTC frequency is determined by an external source via EXT TIME REF etched pad on module.

***Factory-jumpered configuration**

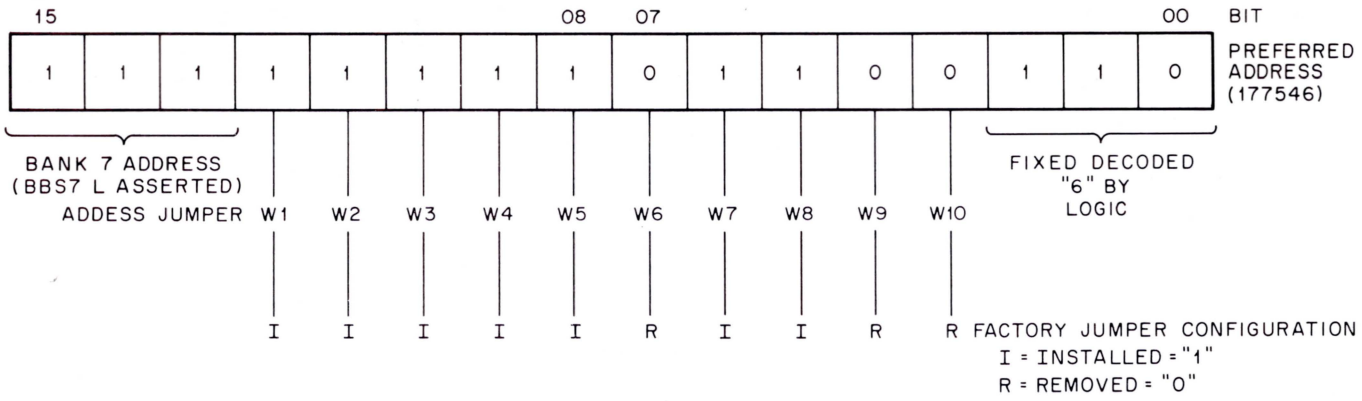


Figure 6. KPV11 Device Address (LKS Register) Jumpers

INSTALLING THE KPV11

Installation In The LSI-11 Backplane

The KPV11 module can be installed in any LSI-11 structured backplane such as the H9270 and DDV11-B. The KPV11 may be inserted into any option location when not used as a terminator. This option does not require the use of the LSI-11 daisy-chained grant signals (BIAK L and BDMG L), and is not priority dependent upon device position in the backplane.

When used as a terminator (KPV11-B and KPV11-C), the module is inserted in the last available option location in the DDV11-B single backplane or H9270 multiple backplane system. Refer to Optional Bus Terminations for more information.

When the optional Console Panel is used with terminator option and the RUN indicator is desired, the following must be performed:

- The KPV11 module must be inserted in the last option location in the H9270 or DDV11-B backplane system.
- Connect a wire* on the backplane from pin CH1 or AH1 on the KPV11 module to the S RUN L signal on the processor module. This signal is located on pin CH1 of the KD11-F processor.

Remote Installation

The KPV11 can be mounted in a remote location (not installed in a backplane) if desired. Mounting holes are provided in the module for this purpose. Mounting details (mechanical) are shown in Figure 7.

NOTE

Program control of the LTC function is not possible when remote installation is used. However, manual control via the optional console panel is available.

Electrical connection between the KPV11 module and the LSI-11 bus is made via a 10-pin connector (J2) on the KPV11 and a 10-pin connector on the backplane (H9270 or DDV11-B) in which the LSI-11 processor is installed. The optional signal cable (DEC Part No. 70-12754) provides the electrical connection between the two 10-pin connectors.

The +5 V and +12 V dc voltage sense input must be provided by the user when the KPV11-A is not installed in an LSI-11 backplane.

***The wire must not exceed the length of the LSI-11 Bus.**

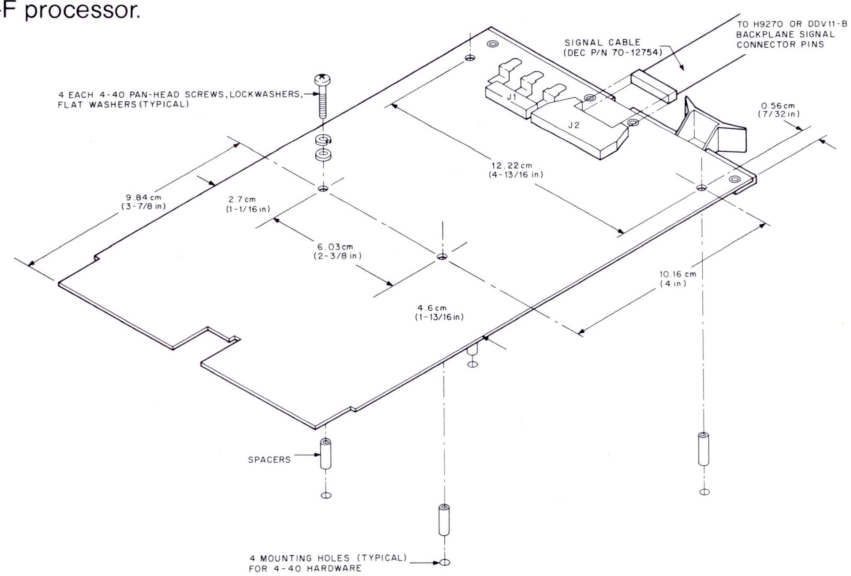


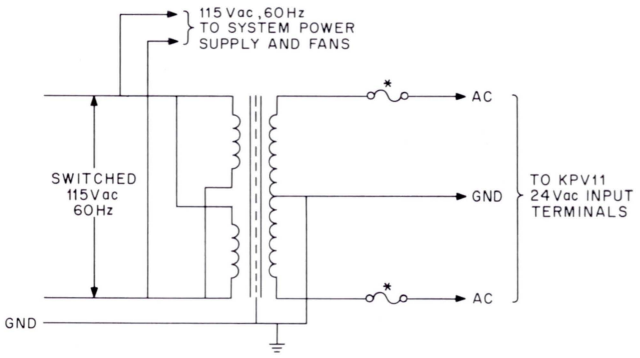
Figure 7. KPV11 Remote Installation

Etched pads are provided on the KPV11-A module for this purpose and are located as shown in Figure 5. Connect the +5V, +12V, and GND pads to the respective LSI-11 backplane power terminals.

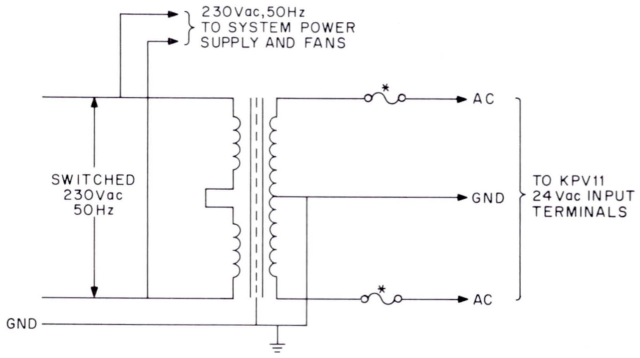
If the optional console panel is to be used, and the RUN indicator function is desired, a wire must be installed between the SRUN L pin (pin 3) on the 10-pin connector on the backplane and processor module pin CH1.

Power Sense Connections

Three tabs on the KPV11 are provided for connecting the option to a 24 Vac center-tapped transformer. This 50 or 60 Hz input voltage produces the required dc operating voltages for the option, provides the 50 or 60 Hz reference for the LTC function, and is the power fail monitor signal for the power signal sequence circuit. This voltage must be supplied by the user. A transformer can be connected as shown in Figure 8 for this purpose. When the KPV11 is used with a 50 Hz input voltage, resistors R35 and R54 must be removed for proper power fail time to compensate for the change in frequency. The location of these resistors are shown in Figure 5.



(A) 115V CONNECTIONS (TYPICAL)



(B) 230V CONNECTIONS (TYPICAL)

Figure 8. Power Line Monitor Transformer Installation

***1 amp fast blow fuses are recommended on the AC input lines to provide adequate protection to the KPV11.**

INSTALLING THE CONSOLE PANEL

The optional console panel can be mounted as shown in Figure 9. Electrical connections between the KPV11 and the console panel are made via 16-pin dual-in-line integrated circuit sockets located on each assembly. The electrical connection between the sockets is made using a signal/power cable (DEC Part No. 70-086 12-0D).

In addition to the LTC ON/OFF and RUN/ENABLE switch functions, the console panel includes a DC ON/OFF switch. This switch, when in the OFF position, disables BDCOK H and BPOK H signal generation. If desired, this switch can also control the DC ON/OFF state of the user's power supply. This function is enabled by connecting the REMote DC ON/OFF and GND etched pads on the KPV11 module to an appropriate control circuit in the power supply. The signal thus produced is TTL compatible and is capable of sinking 16 mA signal current in its logical low (DC ON) state. The logical high state is the DC OFF condition.

USING AN EXTERNAL TIME REFERENCE

The KPV11 normally uses the 50 or 60 Hz input (via the three power tabs on the module) for LTC signal generation. However, an external frequency source may be used for producing LTC signals at frequencies other than the power line frequency. An etched pad is provided for this purpose on the KPV11 module. First, cut or remove jumper W15; this jumper and the EXternal Clock pad are located as shown in Figure 5. Then, connect the external frequency source to the EX CL and GND pads. The frequency source must be TTL logic-compatible; the KPV11 presents three TTL loads to the source.

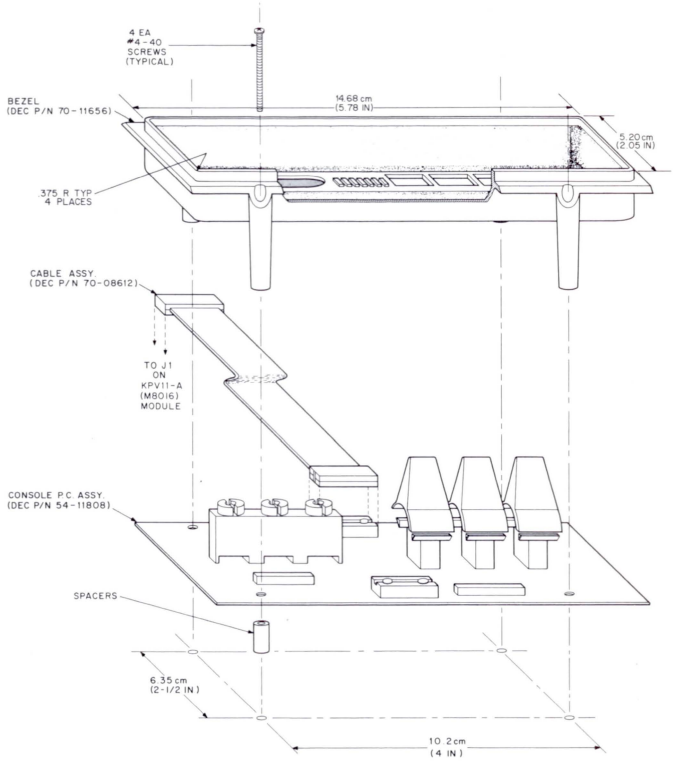


Figure 9. Console Panel Installation

PROGRAMMING

Power Down and Power Up Routines

Power down and power up routine examples for LSI-11 systems using core memory are provided below. The power down routine shown below provides an orderly power down sequence of the system and saves the contents of the general purpose registers along with the stack pointer and the processor status word. Other device registers which the user desires saved during power down can be included through the use of the MOV @ NAME—(SP) instruction.

The power down routine is entered via the routine's starting address ($PWRDN) in interrupt vector location 24; location 26 should contain 200_8 to disable device interrupts during the power down sequence. The first MOV instruction temporarily replaces the power down vector address with the address of a HALT instruction ($HLT). This prevents an erroneous power-up attempt during the power down routine execution. A sequence of MOV instructions then saves register contents on the stack. The second from the last MOV instruction, however, saves the SP in location $SAVR6 which is dedi-

Power Down Routine Programming Example

```
$PWRDN:   MOV     #$HLT,@#24      ;Disable false
                                  ;restart sequence
          MOV     R0,—(SP)        ;PUSH R0 ON STACK
          MOV     R1,—(SP)        ;PUSH R1 ON STACK
          MOV     R2,—(SP)        ;PUSH R2 ON STACK
          MOV     R3,—(SP)        ;PUSH R3 ON STACK
          MOV     R4,—(SP)        ;PUSH R4 ON STACK
          MOV     R5,—(SP)        ;PUSH R5 ON STACK
          MOV     @NAME,—(SP)     ;SAVE ANY NECESSARY DEVICE
                                  ;REGISTERS
          MOV     SP,$SAVR6       ;SAVE SP
          MOV     #$PWRUP,@#24    ;Set power-up vector
$HLT:     HALT                    ;Power down sequence
                                  ;done, Ready for
                                  ;power-up sequence.
$SAVR6:   .WORD 0                 ;SP saved here
```

Power Up Routine

```
$PWRUP:   MOV     #$ILLUP,@#24    ;SET FOR FAST DOWN
          MOV     $SAVR6,SP       ;GET SP
          MOV     (SP)+,@NAME     ;RESTORE ANY DEVICE REGISTERS
                                  ;SAVED
                  Restore any Device
                        .               .
                        .               .
                        .               .
          MOV     (SP)+,R5        ;POP STACK INTO R5
          MOV     (SP)+,R4        ;POP STACK INTO R4
          MOV     (SP)+,R3        ;POP STACK INTO R3
          MOV     (SP)+,R2        ;POP STACK INTO R2
          MOV     (SP)+,R1        ;POP STACK INTO R1
          MOV     (SP)+,R0        ;POP STACK INTO R0
          MOV     #$PWRDN,@#24    ;SET UP THE POWER DOWN VECTOR
          TYPE                    ;REPORT THE POWER FAILURE
$PWRMG:   .WORD   $POWER          ;POWER FAIL MESSAGE POINTER
          RTI
$ILLUP:   HALT                    ;THE POWER UP SEQUENCE WAS
                                  ;STARTED
          BR      .2              ;BEFORE THE POWER DOWN WAS
                                  ; COMPLETE
$SAVR6:             0             ;PUT THE SPHERE
$POWER:   .ASCIZ    <15><12>"POWER"
```

cated by the program for this purpose. It is the last register saved by the routine. The starting address ($PWRUP) for the power-up routine is then written into location 24, replacing the temporary $HLT address. Finally, the program halts and the power down sequence is completed.

When power is restored, the power-up routine is entered via the routine's starting address ($PWRUP) in interrupt vector location 24. The power-up routine, shown below, uses the $HLT and $SAVR6 locations shown in the power-down routine for disabling false power down sequences and restoring the stack pointer, respectively. The first two MOV instructions reference those locations. A sequence of MOV instructions that follow restore device and processor registers, respectively. The last MOV instruction writes the starting address ($PWRDN) for the power fail routine in location 24, replacing the temporary $HLT address. Finally, the RTI instruction pops the PC and PS of the program where the power down sequence occurs from the stack and normal program execution is restored.

Programming the LTC

The LTC function normally divides time into 16⅔ msec or 20 msec intervals determined by the line frequency source (60 Hz or 50 Hz, respectively). It is possible to disable the line frequency source and use an external frequency source (user-supplied). The LSI-11 program communicates with the LTC function via the LKS register (Figure 10) contained in the KPV11 logic circuits. The LKS register's device address is normally configured to 177546 for system software compatibility.

LTC interrupts, when enabled (LKS bit 06 = 1), occur as an interrupt request (bus low assertion) on the BEVNT L signal line. This causes the processor to execute a service routine via vector address 100. Memory location 100 must contain the PC (starting address) for the LTC service routine; similarly, memory location 102 must contain the PS (processor status word) for the service routine. As with all "external" interrupts, the LSI-11 processor will recognize the LTC interrupt request only when the current PS bit 07 is cleared. When PS bit 07 = 1, external interrupts, including the LTC interrupt, are ignored. The LTC interrupt has highest

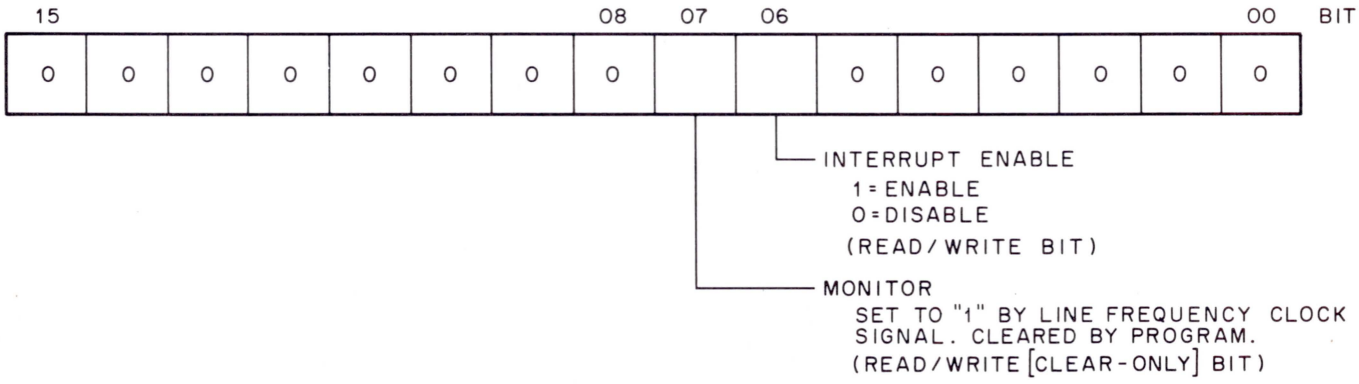


Figure 10. Line Time Clock Status Register (LKS)

priority of all external interrupts and does not require a vector address bus transfer. An interrupt request via the BEVNT L bus signal line, as previously stated, always results in access to the service routine via vector address 100.

The KPV11 is factory-configured for programmable operation as described above. If the user's hardware configuration also includes the optional console panel, the operator can disable or enable the LTC function by setting the LTC ON/OFF switch to the desired position. When set to the OFF position, the LTC switch overrides program control and LTC operation is disabled. W14 must be installed for this function.

CONSOLE OPERATION

The console panel option controls and indicators are shown in Figure 11 and described below:

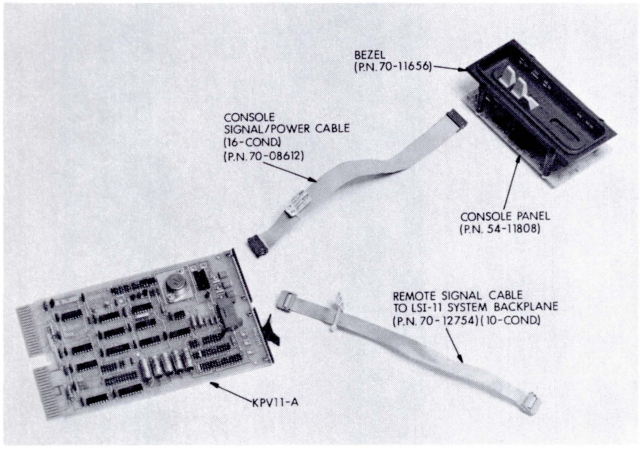


Figure 11. Console Panel Controls and Indicators

Control/ Indicator	Type	Function
DC ON	LED indicator	Illuminates when the DC ON/OFF toggle switch is set on ON and proper dc output voltages are being produced by the user's power supply and sensed by the KPV11. If either the +5V or +12V output from the power supply is faulty, the DC ON indicator will not illuminate.
RUN	LED indicator	Illuminates when the LSI-11 processor is in the run state or the CPU is "hung" (see ENABLE/HALT).
Spare	LED indicator	
DC ON/OFF	Two-position toggle switch	When set to ON, enables the dc outputs of the user's power supply (if connected for this function—see instruction for installing the console panel). The DC ON indicator will illuminate if the dc output voltages are of proper values. When set to OFF, the power supply dc outputs are disabled and the DC ON indicator is extinguished.
ENABLE /HALT	Two-position toggle switch	When set to ENABLE, the B HALT L line to the processor is not asserted and the processor is in the run—enable mode (RUN indicator is illuminated only when the processor is executing a program). When set to HALT, the B HALT L line is asserted. The processor halts program execution and executes console ODT microcode. The RUN indicator is extinguished. If when set to HALT, the RUN light remains illuminated, the CPU is in a "hung" condition. Verify that system memory jumpers/ switches are set up properly.
LTC ON/OFF	Two-position toggle switch	When set to ON, enables KPV11 generation of LTC interrupts. When set to OFF, disables LTC interrupts (W14 must be installed).

TECHNICAL DESCRIPTION

General

Two main functions are contained on the KPV11 module —power signal sequence circuits and programmable line time clock circuits. In addition, the KPV11 interfaces the console panel option to the LSI-11 system.

Power Signal Sequence Circuits

Operating Power—Power signal sequence circuits are shown in Figure 12. Operating power for these circuits is obtained from the 24 Vac, 50 Hz or 60 Hz input at the two ac terminals and GND. Conventional full-wave rectifiers produce +17 V and −17 V operating voltages for the ac line monitor Schmitt trigger (Q1 and Q2) and a 5 V three-terminal regulator; the regulated +5 V is distributed throughout the power signal sequence circuit for operating power.

Power Up—During the power up sequence, ac voltage from the transformer secondary is applied to a Schmitt trigger circuit (Q1 and Q2). The Schmitt trigger squares the ac sine-wave and drives level converter Q3. Q3's output is a TTL-compatible signal. The square wave signal is applied to two 10 msec (nominal) one-shots (and the LTC circuits). One one-shot triggers on the positive-going transition of the square wave signal and the other triggers on the negative-going transition. The one-shot outputs are OR'ed, producing a high (normal) output at gate E6-13. Normally, one one-shot or the other will be in the set state. If a transition of the square wave signal is not followed by a transition of the opposite polarity within 20 msec both one-shots will time out and the logic signal at E6-13 will go low; this is a power fail condition.

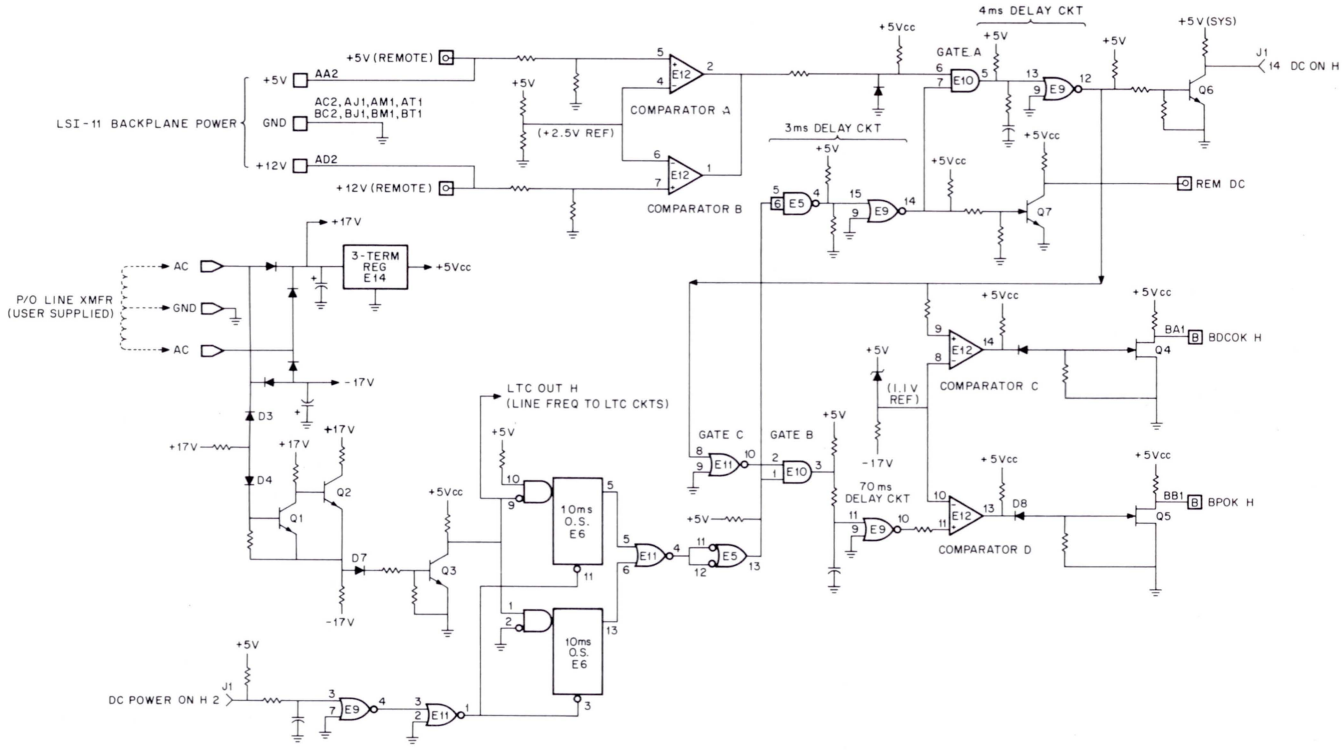


Figure 12. Power Signal Sequence Circuits

During a power up sequence, voltage sense +5V and +12V (remote sense), or +5V and +12V (LSI-11 backplane voltages), inputs rise to voltage levels that cause voltage comparators A and B to produce high outputs. The comparator outputs are connected together and applied to one input of gate A. The remaining input of gate A is enabled by the normally high gate E6-13 signal, which is applied (but not delayed) via the 3 msec delay circuit. Gate A's output goes high. This signal is then delayed 17 msec and inverted, producing a low signal which is applied to the non-inverting input of comparator C and gate C. Comparator C's output goes low, turning off Q4 and producing an active BDCOK H signal 17 msec (minimum) after ac power is applied.

Gate C's output goes high enabling gate B. The remaining gate B input is enabled by the high gate E6-13 output signal. Gate B's high output signal is delayed 70 msec and inverted, producing a low signal (E10-10) which is applied to the non-inverting input of comparator D. Comparator D's output signal goes low, turning off Q5, and producing the active BPOK H signal 70 msec after the active BDCOK H signal. With both signals in the active (high) state, normal system operation can proceed.

Power Down—When an ac power failure occurs, the trigger pulses to the one-shots cease, and both one-shots time out. Gate E6-13 goes low, inhibiting gate B, and initiating the 3 msec delay (E6-4 signal voltage starts to rise from the logical low state). Gate B's output goes low; this low signal is inverted, but not delayed, by the 70 msec delay circuit, and the resulting high signal is applied to the non-inverting input of comparator D. Comparator D's output goes high, turning on Q5, and negating BPOK H. Meanwhile, the 3 msec delay circuit, after the 3 msec delay, produces a low signal at E10-14. A low signal inhibits gate A causing its output signal to go low. The low signal inhibits gate A causing its output signal to go low. The low signal is inverted (but not delayed) by the 17 msec delay circuit, and applied to the non-inverting input of comparator C. Comparator C's output goes high, turning on Q4 and negating the BDCOK H signal 3 msec after BPOK H becomes negated. Q6 monitors the 17 msec delay circuit output and produces the DC ON H signal for the remote console panel display. When dc voltages are normal, E10-12 goes low; Q6 cuts off and DC ON H goes high. When dc voltages are not present, E10-12 goes high; Q6 turns on and negates DC ON H.

When the remote console panel is connected to the KPV11, the DC ON/OFF switch can simulate a power line failure and control the user's power supply. The simulated power line failure occurs when a low DC POWER ON H occurs (DC OFF switch position). This low signal produces a low signal that clears both one-shots, and the simulated power failure results.

Remote control of the user's power supply is made possible via the REMote DC ON/OFF etched pad. The signal present at this point is the 3 msec delay circuit signal (E10-14) inverted by Q7. Thus, when normal line voltage is sensed, and the remote console panel DC ON/OFF switch is not in the Off position, this signal goes low, activating a control circuit in the user's power supply that turns dc voltages on. When this signal is high—a result of power fail or placing the remote console panel DC ON/OFF switch in the Off position—the user's power supply dc output voltages should turn off.

Programmable Line Time Clock Circuits

Programmable line time clock functions are shown in Figure 13. Jumpers allow selection of line frequency or external time base operation, console LTC ON/OFF switch enable/disable, and manual/programmable operation. Additional jumpers (W1-W10) select the device address for the LKS register. Jumpers are factory-configured as shown in the figure.

Program access to the LKS register is via the address configured via jumpers W1-W10. The processor first places the KPV11 LKS register address on BDAL <00:15> L and asserts BBS7 L. Note that BBS7 L is asserted only during an addressing operation when BDAL 13:15 L are asserted; hence, the address decoders receive only BDAL 00:12 L and BBS7 L. Device selection occurs on the leading edge of BSYNC L. If the address input matches the jumpered address, LKS H goes high (true), and remains true for the duration of the LSI-11 bus cycle.

Two flip-flops comprise the two significant bits of the LKS register. Bit 06 is produced by the LTC ENaBle flip-flop. Similarly, bit 07 is produced by the LTC MONitor flip-flop.

During a programmed write operation (DATO, DATOB, or the write portion of DATIO, or DATIOB bus cycle), LKS L (LKS H inverted) and BDOUT L are AND'ed to produce an active (high) WRITE LKS H signal. The leading edge of LKS H clocks the logical state of RDAL06 H into the LTC ENB flip-flop, enabling or disabling LTC interrupts. The LTC MON flip-flop, however, can only be preset during the write cycle. Note that the LTC MON flip-flop, when preset, is read as a logical 0 via the flip-flop's Q output; when the flip-flop is reset, it is read as a logical 1. RDAL07 L (0 = high) is AND'ed with WRITE LKS H, producing a low signal that presets the flip-flop; MONITOR H then goes low.

Normally, the LTC ON/OFF input to E10-5 is passive (high), producing a low at E10-6 that enables AND gate input E13-12. When interrupts are enabled, LTC ENB(1) L enables E13-11 and E13-13 goes high. This signal then enables one input of the BEVNT L bus driver. The remaining bus driver input is the LTC H signal. Thus, when LTC H goes high, BEVNT L goes low, and the LTC interrupt request is presented to the LSI-11 processor.

The leading edge of LTC H also clocks the LTC MON flip-flop to the reset state and MONITOR H goes true (high). MONITOR H conditions one input of the BDAL07 H bus driver. During a read cycle (DATI, or the read portion of the DATIO cycle), LKS L and BDIN L are gated to produce an active (high) READ LKS H signal. READ LKS H enables both BDAL07 L and BDAL06 L bus drivers, gating the MONITOR and INTERRUPT ENABLE status bits onto the LSI-11 bus.

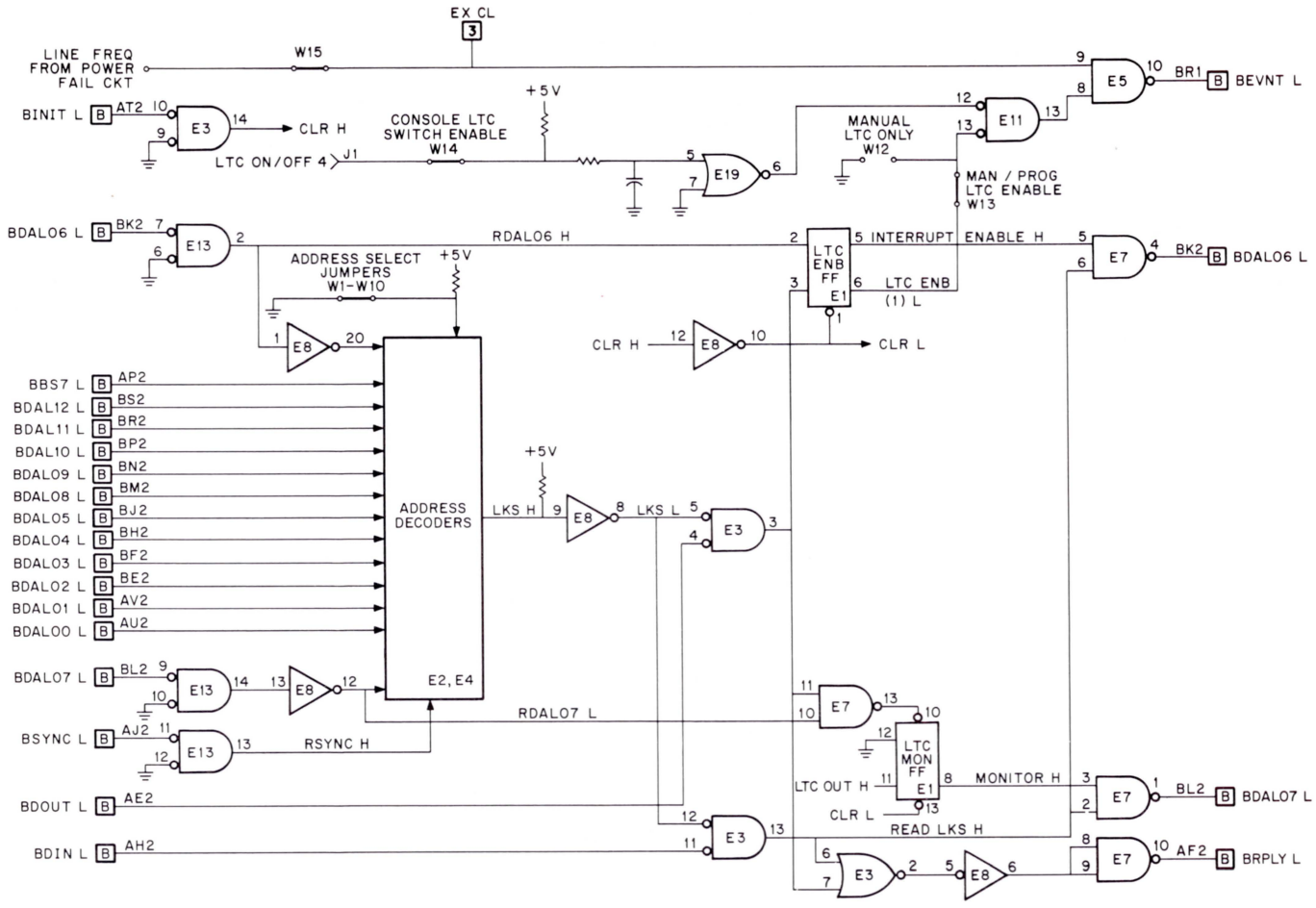


Figure 13. Programmable Line Time Clock Circuits

During both programmed read and write bus cycles, the KPV11 must respond by asserting BRPLY L. READ LKS L and WRITE LKS L are OR'ed and applied to the BRPLY L to produce the appropriate device response according to LSI-11 bus protocol.

The optional console panel includes the LTC ON/OFF switch. When placed in the OFF position, J1-4 is low; E10-6 goes high, inhibiting E13-12 and LTC interrupt requests are disabled. This function can be disabled by removing W14.

When manual-only LTC operation is desired, W13 is removed and W12 is installed. E13-11 is continuously enabled and LTC interrupt requests can be disabled via the console panel LTC ON/OFF switch; W14 must be installed for this operation.

Console Panel Interface

The optional console panel interfaces with the LSI-11 system via the KPV11 module as shown in Figure 15. The DC ON indicator (D1) is directly driven by the DC ON H driver (Q6) in the power signal sequence circuit.

The RUN indicator is driven by the LSI-11 processor-generated SRUN L signal pulse. The 200 msec one-shot receives a continuous series of trigger pulses, when the processor is in the "Run" (program execution) state, that keeps the one-shot in the retriggered state. When in this state, the one-shot produces a high signal that turns on the RUN indicator (D2) via the LED driver. When the processor is halted, the 200 msec one-shot times out, and the RUN indicator extinguishes.

The three console switches each include a "debounce" circuit comprised of cross-coupled inverters. DC ON/OFF and LTC ON/OFF functions are used as previously described for power signal sequence and programmable line time clock circuits, respectively.

The ENABLE/HALT switch enables the run mode (by not asserting BHALT L) or halts the LSI-11 processor; when halted, console ODT microcode operation is invoked, as described in the Microcomputer Handbook. An R-C filter and BHALT L bus driver circuit on the KPV11 module interface this function to the LSI-11 bus.

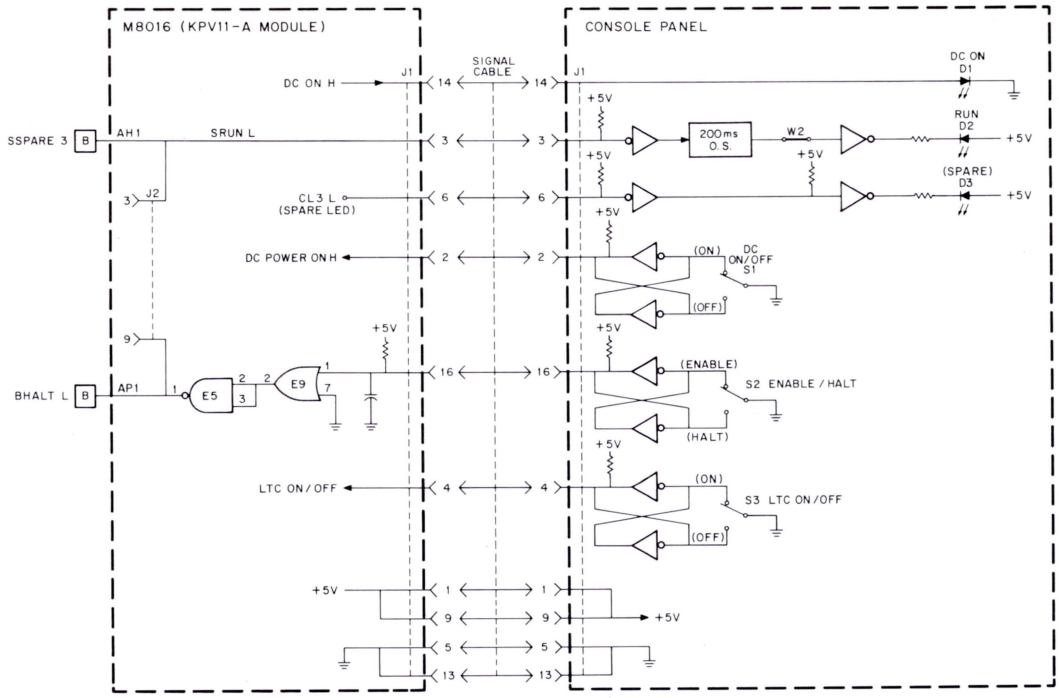


Figure 14. Console Panel Interface

Optional Bus Terminations

Two types of terminations are available as options: The KPV11-B supplied with 120 ohm termination and the KPV11-C supplied with 250 ohm termination. Each bus signal line termination includes two resistors as shown in Figure 15. Termination resistors are contained in 16-pin dual-in-line packages which are physically identical to I.C. packages. Each package contains 14 terminations. Daisy-chained grant signals are jumpered but not terminated. BIAKI L is jumpered to BIAKO L, and BDMGI L is jumpered to BDMGO L. Additional bus termination information is available in the Microcomputer Handbook.

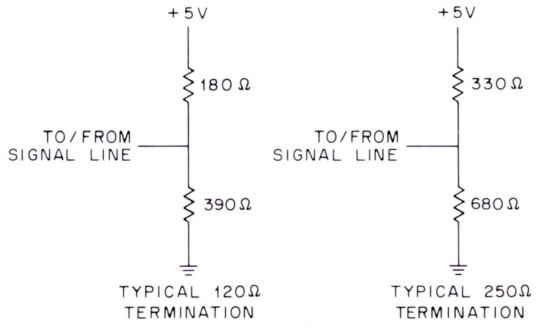


Figure 15. Bus Termination Resistors

WARRANTY

KPV11 (M8016) modules are warranted for a period of one (1) year from date of shipment. Cables and remote console options are warranted for a period of ninety (90) days from date of shipment.

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